Rafael A. Arce-Nazario

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RESEARCH INTERESTS

Custom computing machines built using reconfigurable technology, such as Field Programmable Gate Arrays (FPGAs), can significantly accelerate certain computing tasks. My primary interest centers on designing methodologies for the automated and/or systematic implementation of high-performance algorithms onto custom computing architectures.

EDUCATION

Doctor of Philosophy in Computer and Information Sciences and Engineering
University of Puerto Rico, Mayagüez, PR
Dissertation topic:
High-Level Partitioning of Discrete Signal Transforms for Distributed Hardware Architectures.
PhD Candidate - Expected graduation date: May 2007 GPA: 4.00/4.00

Master of Science in Electrical Engineering, Magna Cum Laude
December 1993 - University of Wisconsin, Madison, WI GPA: 3.93/4.00

Bachelor of Science in Computer Engineering, Magna Cum Laude
June 1992 - University of Puerto Rico, Mayagüez, PR GPA: 3.92/4.00

WORK EXPERIENCE

7/04 – 10/04 **Co-op Circuit Engineer – Engineering and Technology Services, IBM, Rochester, MN.**
As a member of the Chip Physical Design and CAD Tools group, I worked in the analysis and implementation of methods to detect and assess the impact of physical design optimizations on chip routing. I ported several of the existent analysis algorithms to C/C++ for a 10x increase in processing speed and integrated the previously isolated steps of the detection methodology into a completely automated process. The results of using our methods for spotting situations detrimental to routing were documented in a technical paper, presented in the 2005 ACM International Symposium on Physical Design.

8/02 – present **PhD Candidate. Computer and Information Sciences and Engineering Program. University of Puerto Rico, Mayagüez, PR**
Conducting research in the areas of reconfigurable computation and computer aided design for digital systems. Most relevant courses taken: Advanced Algorithms for DSP, VLSI Systems Design, and Analysis of Algorithms, Computer Arithmetic, Advanced IC Design Techniques and Computational Logic. Passed qualifying exams August 2003. Published five technical papers on international peer reviewed conferences.

6/02 – 8/02 **Engineering Intern. Digital ASICs Group. Digital Technology Center. Eastman Kodak, Rochester, NY**
Designed and implemented data paths and algorithms for FPGA PCI board used in digital imaging. Developed C programs to help test and validate the VHDL design. Modified Linux drivers to work with the FPGA board.

8/97 – present (study leave) **Assistant Professor. Department of Physics and Electronics, University of Puerto Rico (UPR), Humacao, PR**
Taught courses in electronics, microprocessors and computer programming. Supervised undergraduate design projects in microprocessors and digital electronics. Wrote proposals for external funding. Conducted Internet and web page seminars for professors, K-12 teachers, and students. Acted as Academic Programs Coordinator and President of the department's Student Recruitment Committee.

8/95 – 5/97 (full time) **Instructor. Statistics and Information Systems Department, UPR, Rio Piedras, PR**
Taught Computer Programming and Information Systems courses.

8/95 – 8/96 (part time) **Instructor. Electrical Engineering Department, Polytechnic Univ. of Puerto Rico, Hato Rey, PR**
Taught Computer Programming and Data Structures courses to engineering students.

1/94 – 5/95 (full time) **Computer Integrated Manufacturing Engineer. Motorola Electrónica de Puerto Rico, Vega Baja, PR**

Developed and maintained Computer Integrated Manufacturing (CIM) applications. Performed system administration and support tasks for Stratus and HP700 systems. Supported PLCs in a manufacturing environment. Designed and implemented computer programs for quality control.

SELECTED PUBLICATIONS AND PRESENTATIONS

- R.. Arce Nazario, M. Jiménez, D. Rodriguez. "Algorithmic-level Exploration of Discrete Signal Transforms for Partitioning to Distributed Hardware Architectures". Submitted to IET Computers & Digital Techniques. August 2006.
- R. Arce Nazario, M. Jiménez, D. Rodríguez. "High-level Partitioning of Discrete Signal Transforms for Multi-FPGA Architectures". 16th IEEE International Conference on Field Programmable Logic and Applications. August 2006. Madrid, Spain.
- R. Arce Nazario, M. Jiménez, D. Rodríguez. "Functionally-aware Partitioning of Discrete Signal Transforms for Distributed Hardware Architectures". 49th IEEE Midwest Symposium on Circuits and Systems. August 2006. San Juan, PR.
- R. Arce Nazario, M. Jiménez, D. Rodríguez. "Effects of High-Level Discrete Signal Transform Formulations on Partitioning for Distributed Hardware Architectures". IEEE on Symposium Field-Programmable Custom Computing Machines. April 2006. Napa, CA
- R. Arce Nazario, M. Jiménez, D. Rodríguez. "An Assessment Of High-Level Partitioning Techniques For Implementing Discrete Signal Transforms On Distributed Hardware Architectures". 48th IEEE Midwest Symposium on Circuits and Systems. August 2005. Cincinnati, Ohio.
- B. Lembach, R. Arce-Nazario, D. Eisenmenger, and C. Wood. "A diagnostic method for detecting and assessing the impact of physical design optimizations on routing". ACM International Symposium on Physical Design. April 2005. San Francisco, CA.
- R. Arce Nazario, M. Jiménez, "High-Level Partitioning Of DSP Algorithms For Multi-FPGA Systems - A First Approach", Proceedings of the Computing Research Conference, Mayagüez, PR, April 2004.
- R. Arce Nazario, M. Jiménez, "Integer Pair Representation for Multiple Output Logic", 47th IEEE Midwest Symposium on Circuits and Systems. December 2003, Cairo, Egypt.
- R. Arce Nazario, M. Jiménez, "Integer Pair Representation for Multiple Output Logic", Proceedings of the Computing Research Conference, Mayagüez, PR, April 2003.
- R. Arce Nazario, "Multisensory Interface to Allow Blind User Access to Graphics", Proceedings of RESNA 1994 Annual Conference, Nashville, Tennessee, RESNA Press.

PROFESSIONAL SOCIETIES

- **College of Engineers and Surveyors of Puerto Rico (CESPR).** Member of the Computer Engineering Institute. Professional Engineer (PE) license #16554**. (**1992 – present)
- **IEEE –** student member (2004 – present)
- **Association for Computing Machinery –** student member (2003 – present)
- **Association of University Professors.** University of Puerto Rico, Humacao Campus. (2000 – 2002)

ACHIEVEMENTS

- Alliances for Graduate Education in the Professoriate - Graduate Fellowship for 01/2007-06/2007
- NSF-EPSCoR Graduate Fellowship 2004-2005 and 2005-2006
- NASA Space Grant Fellowship – 2003-2004
- Honorable Mention for the Ford Foundation Doctoral Fellowship (2003)
- Principal Investigator of research project in the area of Hyperspectral Systems (Remote Sensing) – Sponsored by the Defense Intelligence Agency (Spring 2001).
- Obtained donation of FPGA test boards and software from Xilinx for electronics labs (Fall 2001).
- Wrote proposal to Hewlett Packard for the donation of equipment to modernize electronics labs. The proposal was accepted and granted in Fall 1999. Directed physical and curricular modernization of electronics laboratories (1999-2000).
- Rehabilitation Engineering Society of North America (RESNA) Conference Easter Seal Student Design Competition Award (June 1994).
- University of Wisconsin Advanced Opportunity Fellowship (1993).
- Commencement Ceremony Award for the Most Outstanding Student in Computer Engineering (1992)
- GTE Scholarship (1992)
- National Hispanic Award Scholarship (1988).